Question 1: [5 Marks]

Consider an inverter with the following characteristics.

$V_{TW} = 1V$, $V_M = 2.5V$, $V_{NSH} = 1.5V$, and $V_{NSL} = 1.5V$

A. Draw the voltage transfer curve for this inverter assuming the curve is piecewise linear. Please show all critical voltages on the drawing.
B. Calculate the noise margins and the noise immunities.

$V_{TW} = 1V$, $V_M = 2.5V$, $V_{NSH} = 1.5V$, $V_{NSL} = 1.5V$

a

$$V_{NSH} = V_{OH} - V_M$$

$$V_{OH} = V_{NSH} + V_M = 1.5 + 2.5 = 4\,V$$ $\boxed{V_{OH} = 4V}$

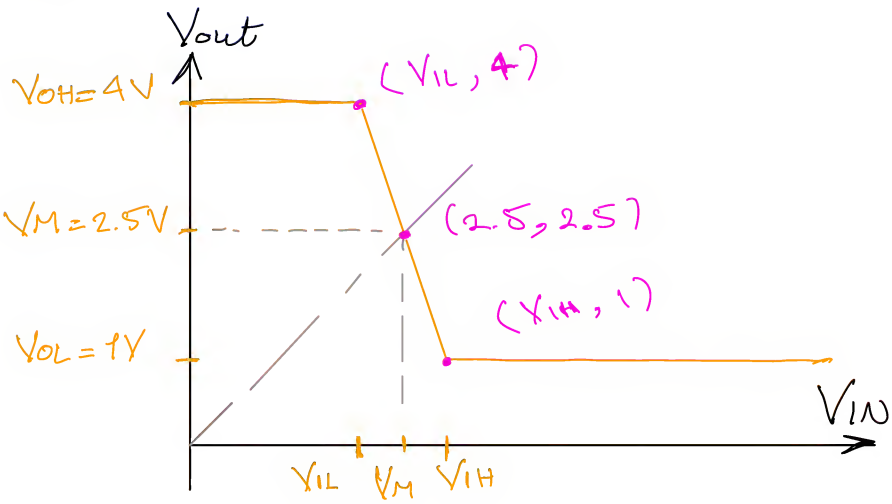
$$V_{NSL} = V_M - V_{OL}$$

$$V_{OL} = V_M - V_{NSL} = 2.5 - 1.5 = 1\,V$$ $\boxed{V_{OL} = 1V}$

$$V_{TW} = V_{IH} - V_{IL}$$

$$V_{IH} - V_{IL} = 1\,V \quad \text{——} (1)$$

Since the VTC curve is piecewise linear



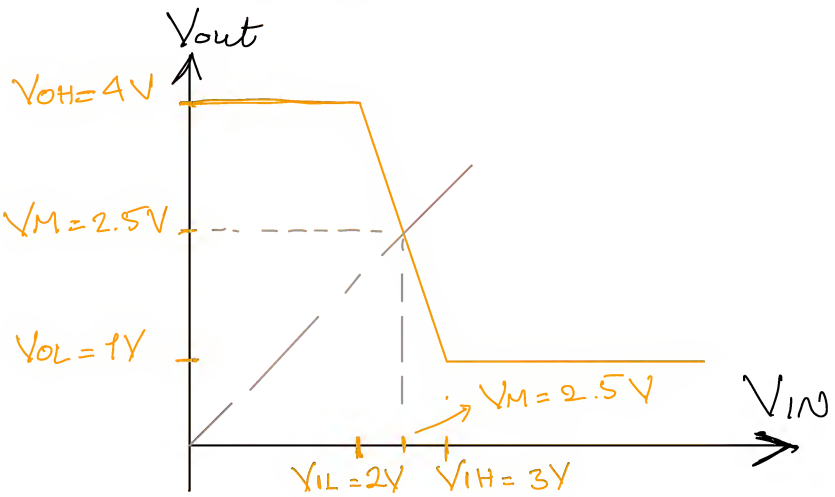
$$\frac{4 - 2.5}{V_{IL} - 2.5} = \frac{2.5 - 1}{2.5 - V_{IH}}$$

$$\frac{1.5}{V_{IL} - 2.5} = \frac{1.5}{2.5 - V_{IH}}$$

$$V_{IL} - 2.5 = 2.5 - V_{IH}$$

$$V_{IH} + V_{IL} = 5\,V \quad \text{——} (2)$$

by solving (1) & (2)



$\boxed{V_{IH} = 3V}$ $\boxed{V_{IL} = 2V}$

b

$V_{NMH} = V_{OH} - V_{IH} = 4 - 3 = 1V$ → $V_{NMH} = 1V$

$V_{NML} = V_{IL} - V_{OL} = 2 - 1 = 1V$ → $V_{NML} = 1V$

$V_{LS} = V_{OH} - V_{OL} = 4 - 1 = 3V$

$V_{NIH} = \frac{V_{NSH}}{V_{LS}} = \frac{1.5}{3} = 0.5$ → $V_{NIH} = 0.5$

$V_{NIL} = \frac{V_{NSL}}{V_{LS}} = \frac{1.5}{3} = 0.5$ → $V_{NIL} = 0.5$

Question 2: [5 Marks]

A. List and explain three uses of diodes.
B. Design a level shifted AND gate using only diodes and resistors. The gate must conform to the following specifications,

Fan-in = 3, P (OL) = 50.9mW, P (OH) = 17.3mW, V_{CC} = 5V, and V_{EE} = 5V

a

* Varactor Diodes: These diodes used to utilize The PN Junction capacitance in ICs. For this device the forward diode voltage V_D is negative.

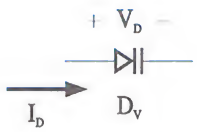


FIGURE 2.4 Varactor Diode (*Voltage Dependent Capacitor* for $V_D < 0$)

* Clamping diodes: Connecting diodes to each input of a gate reduces the input voltage swings (ringing) & therefore protect the gate from physical damage.

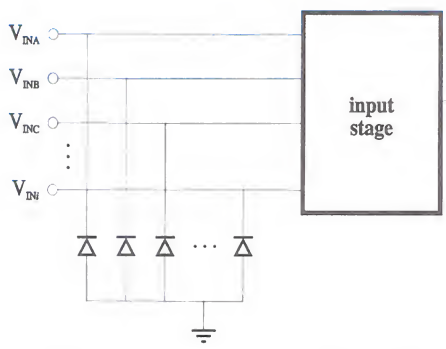


FIGURE 2.10 Input Clamping Diodes

* Level-shifting diodes: It is used to change the voltage level across particular portions of digital circuits. for example it can be used to level shift the output voltage level. Another use is to ensure that sub-circuits with complementary objectives are not conducting simultaneously.

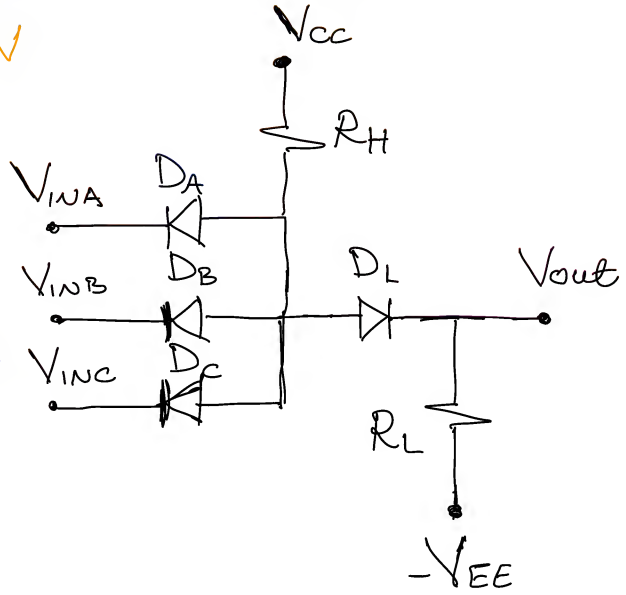
(b)

Fan-In = 3 $P(OL) = 50.9\,mW$ $P(OH) = 17.3\,mW$

$V_{CC} = 5\,V$ $V_{EE} = 5\,V$

* To design means to find the resistors values

* Since there is no mention of the fan-out then for simplicity we'll assume these specification mesured with no loads ($N = 0$)

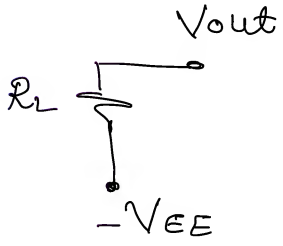


* Any Input low (V_{IH})

D_L is off & Vout is high (V_{OH})

if $V_{IN} = V_{IH} \Rightarrow V_{out} = V_{OH}$

$V_{OH} = -V_{EE} = -5V$



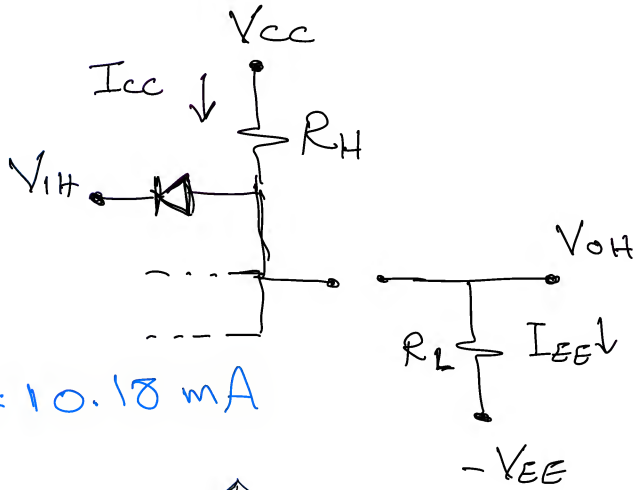
$P(OL) = P_{CC(OL)} + P_{EE(OL)}$

$= I_{CC(OL)} V_{CC} + I_{EE(OL)} V_{EE}$

$I_{EE} = 0 \Rightarrow P_{EE(OL)} = 0$

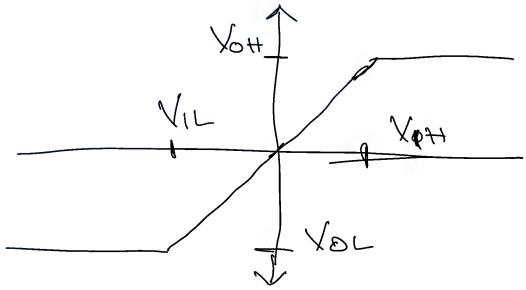
$P(OL) = I_{CC(OL)} V_{CC}$

$I_{CC(OL)} = \frac{P(OL)}{V_{CC}} = \frac{50.9\,m}{5} = 10.18\,mA$



According to the VTC of level-shifted AND gates

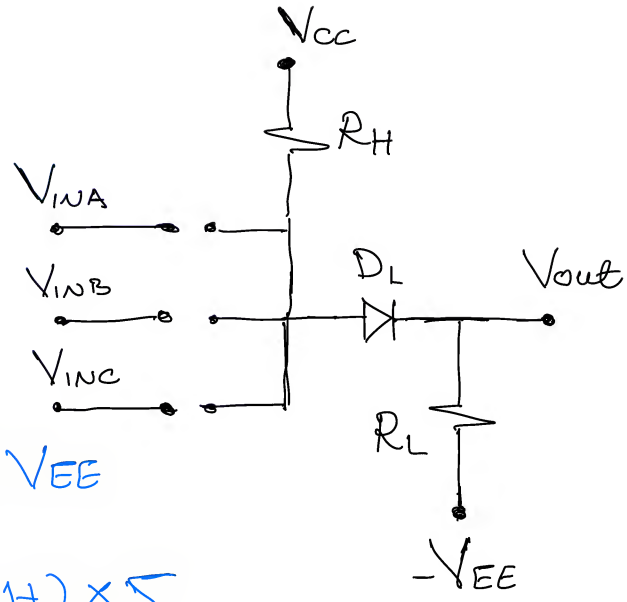
$V_{IH} = V_{OH} = -5\,V$



$$I_{CC(OL)} = \frac{V_{CC} - V_{D(ON)} - V_{IH}}{R_H}$$

$$R_H = \frac{5 - 0.7 + 5}{10.18\,m} = 913.6\ \Omega$$

$$\boxed{R_H = 913.6\ \Omega}$$



* All input high

$V_{IN} = V_{IH} \Rightarrow V_{out} = V_{OH}$

$P_{(OH)} = P_{CC(OH)} + P_{EE(OH)}$

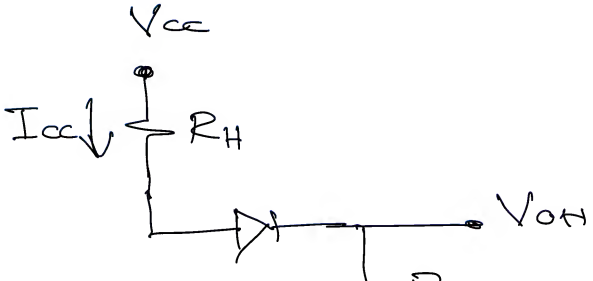
$P_{(OH)} = I_{CC(OH)} V_{CC} + I_{EE(OH)} V_{EE}$

$17.3\,m = I_{CC(OH)} \times 5 + I_{EE(OH)} \times 5$

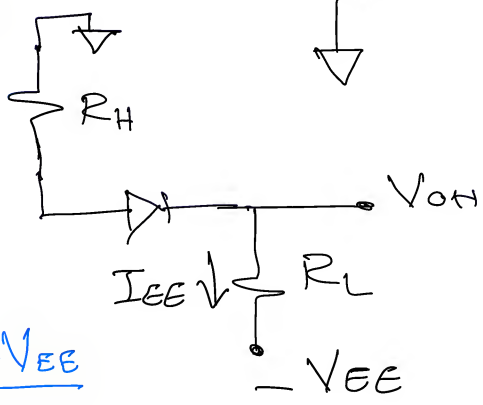
$$I_{CC(OH)} + I_{EE(OH)} = \frac{17.3m}{5} = 3.46\ mA$$

* To find $I_{CC(OH)}$ & $I_{EE(OH)}$ we will use super position theorm

$$I_{CC(OH)} = \frac{V_{CC} - V_{D(ON)}}{R_H + R_L} \quad \text{— (1)}$$



$$I_{EE(OH)} = \frac{0 - V_{D(ON)} + V_{EE}}{R_H + R_L} \quad \text{— (2)}$$



By Adding (1) & (2)

$$I_{CC(OH)} + I_{EE(OH)} = \frac{V_{CC} - 2V_{D(ON)} + V_{EE}}{R_H + R_L}$$

$$R_H + R_L = \frac{5 - 2(0.7) + 5}{3.46m}$$

$$R_L = \frac{5 - 2(0.7) + 5}{3.46m} - 913.6 = 1.572k\Omega$$

$$\boxed{R_L = 1.572k\Omega} \qquad \boxed{R_H = 913.6\Omega}$$

Question 3: [4 Marks]

A. List and compare three different types of integrated resistors.
B. Draw cross section of oxide isolated pinch resistor.

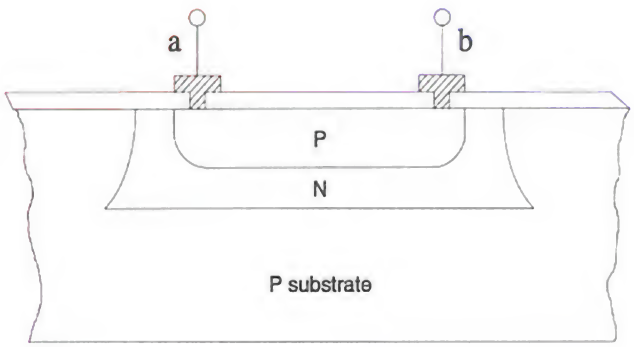
a

① Diffused Base Resistor

* Using the base diffusion/implant region

$$R_{ab} = \rho_{SB} \frac{L}{W}$$

$\rho_{SB} \equiv$ sheet resistivity



* ρ_{SB} of this region is comparatively large and is useful for large IC resistors.
* Typically $\rho_{SB} = 200\Omega/square$.

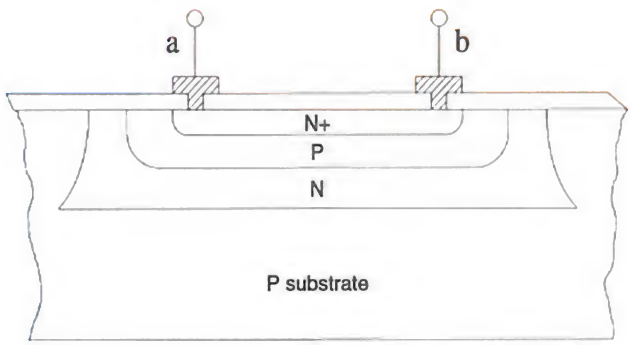
$$\rho_{SB} = \frac{\rho}{t}$$

$t \equiv$ tickness

② Diffused Emitter Resistor

* Using the emitter N^+ region for the resistor

$$R_{ab} = \rho_{SE} \frac{L}{W}$$



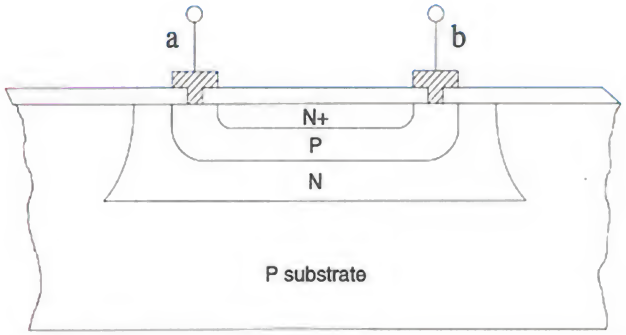
* Typically $\rho_{SE} = 2\Omega/square$.
* This resistor used for small valued resistors

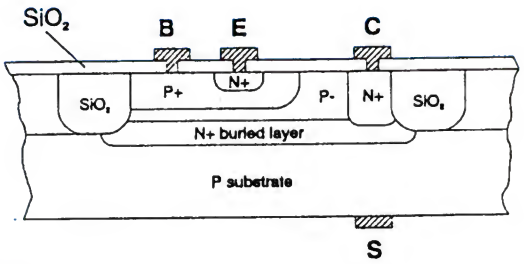
③ Pinch Resistor

* It has the largest value of resistance for a fixed length/width ratio of any of the IC resistors. Because the cross section of the pinch resistor has been reduced by N+ diffusion
* The reduced cross-section has the effect of increasing the sheet resistivity and hence resistor value

$$R_{ab} = \rho_{SB} \frac{L}{W}$$

b

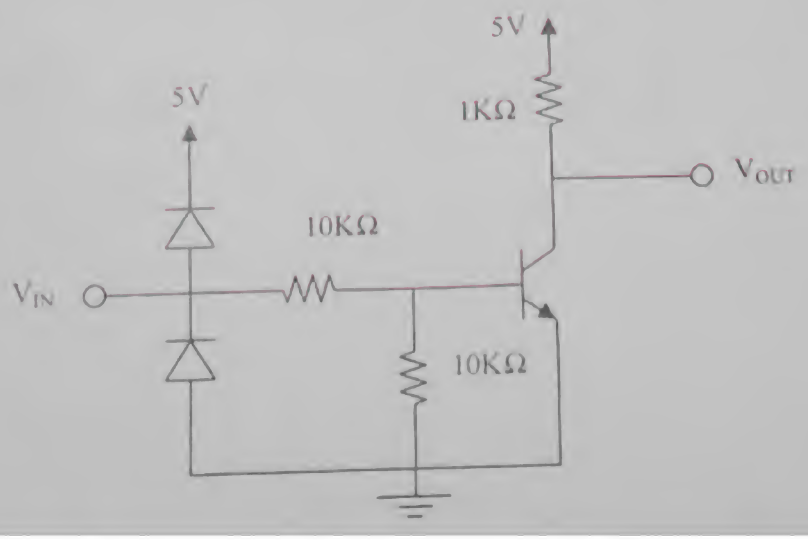




Question 4: [6 Marks]

Consider the following NOT gate. Assume $V_{BE}(SAT) = 0.8V, V_{CE}(SAT) = 0.2V, \sigma = 0.5$, and $\beta_F = 80$
Find the following.

a) Draw the voltage transfer curve
b) Calculate the maximum fan-out
c) Find the average power dissipation with fan out of three



(a) Output high voltage $= V_{OH}$

when The input is low Q is off

$V_{out} = 5 = V_{OH}$

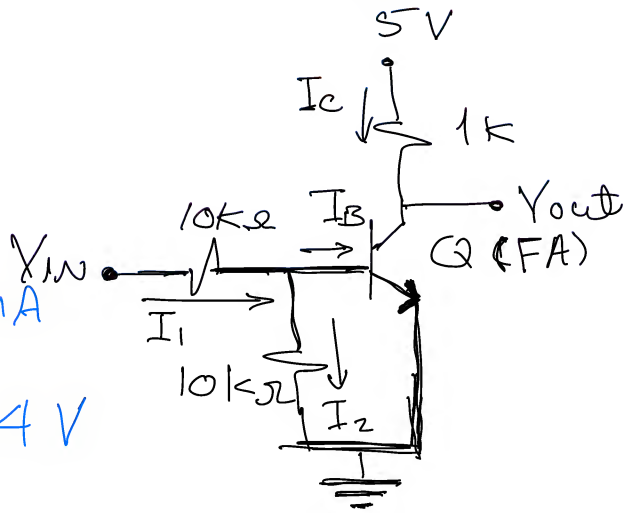
$V_{OH} = 5\ V$

Input low voltage $= V_{IL}$

when V_{IN} reach $V_{BE(FA)}$ Q reach the edge of conduction

$V_{IL} = 10K\ I_1 + V_{BE(FA)}$

@ edge of conduction:



$I_1 = I_2 = \frac{V_{BE(FA)}}{10K} = \frac{0.7}{10K} = 0.07mA$

$V_{IL} = 10K \times 0.07m + 0.7 = 1.4\ V$

$V_{IL} = 1.4V$

Output low voltage $\equiv V_{OL}$

Vout reach the lowest value when Q enters the saturation region

$V_{OL} = V_{CE(sat)} = 0.2V$

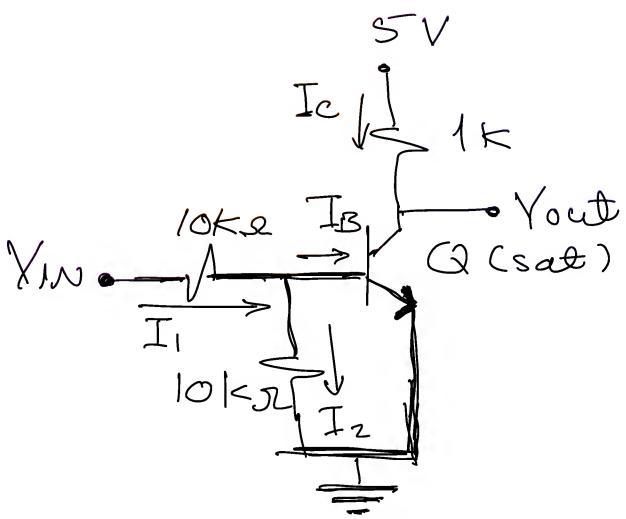
$V_{OL} = 0.2V$

Input high voltage $\equiv V_{IH}$

$V_{IH} = 10K\ I_1 + V_{BE(sat)}$

$I_1 = I_2 + I_{B(sat)}$

$I_{C(sat)} = \beta_f\ I_{B(sat)}$



@ edge of saturation $\sigma = 1$

$$I_{B(sat)} = \frac{I_{C(sat)}}{\beta_f}$$

$$I_{C(sat)} = \frac{5 - V_{CE(sat)}}{1K} = \frac{5-0.2}{1K} = 4.8\,mA$$

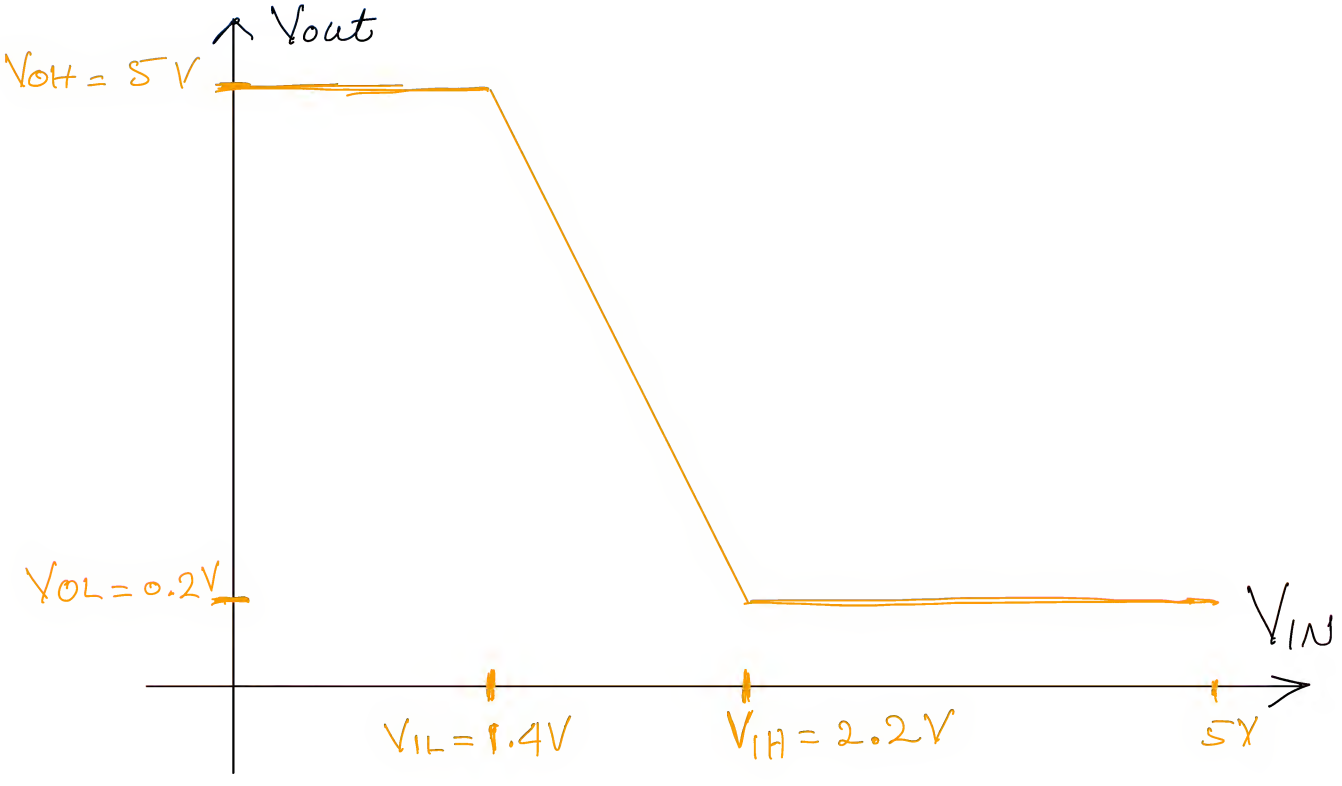
$$I_{B(sat)} = \frac{4.8\,mA}{80} = 0.06\,mA$$

$$I_2 = \frac{V_{BE(sat)}}{10K} = \frac{0.8}{10K} = 0.08\,mA$$

$$I_1 = 0.08m + 0.06m = 0.14\,mA$$

$$V_{IH} = 10K \times 0.14m + 0.8 = 2.2\,V$$

$$\boxed{V_{IH} = 2.2V}$$

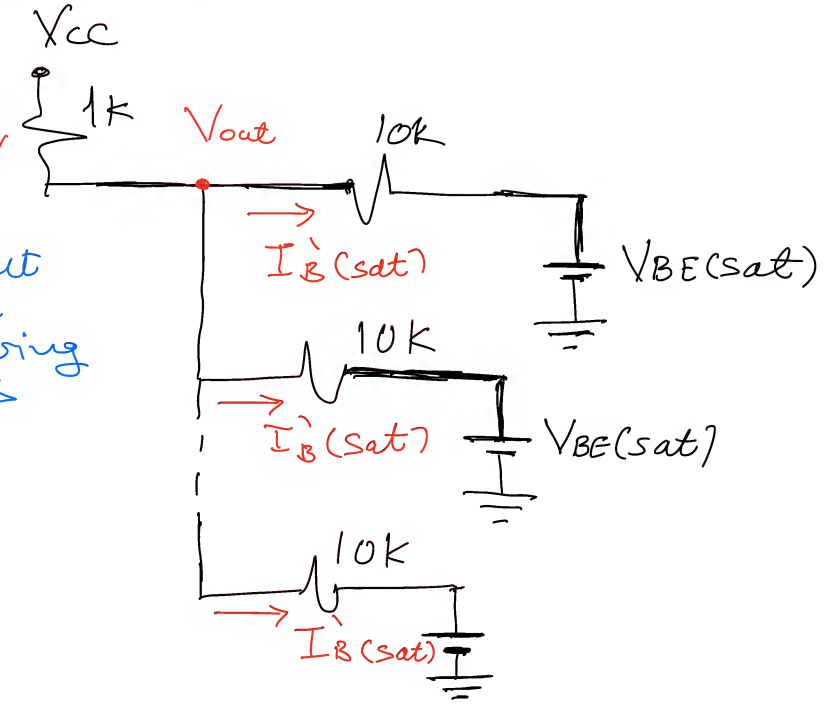


b

$N_{max} = \min(N_{high}, N_{low})$

* N_{high}

$I_{CC(OH)} = N I'_{B(sat)}$



For maximum fan-out Vout must be the minimum voltage enough to saturate the driving gate transistor which is

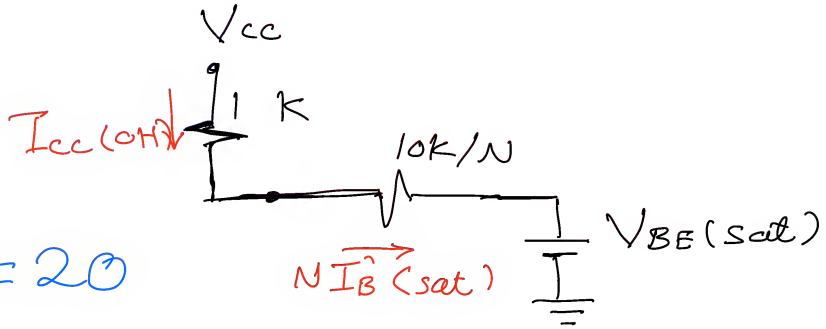
$V_{OH(min)} = V_{IH}$

$I_{CC(OH)} = \frac{V_{CC} - V_{IH}}{1K}$

$I'_{B(sat)} = \frac{V_{IH} - V_{BE(sat)}}{10K}$

$N = \frac{V_{CC} - V_{IH}}{V_{IH} - V_{BE(sat)}} \left(\frac{10K}{1K}\right)$

$= \frac{5 - 2.2}{2.2 - 0.8} \left(\frac{10K}{1K}\right) = 20$

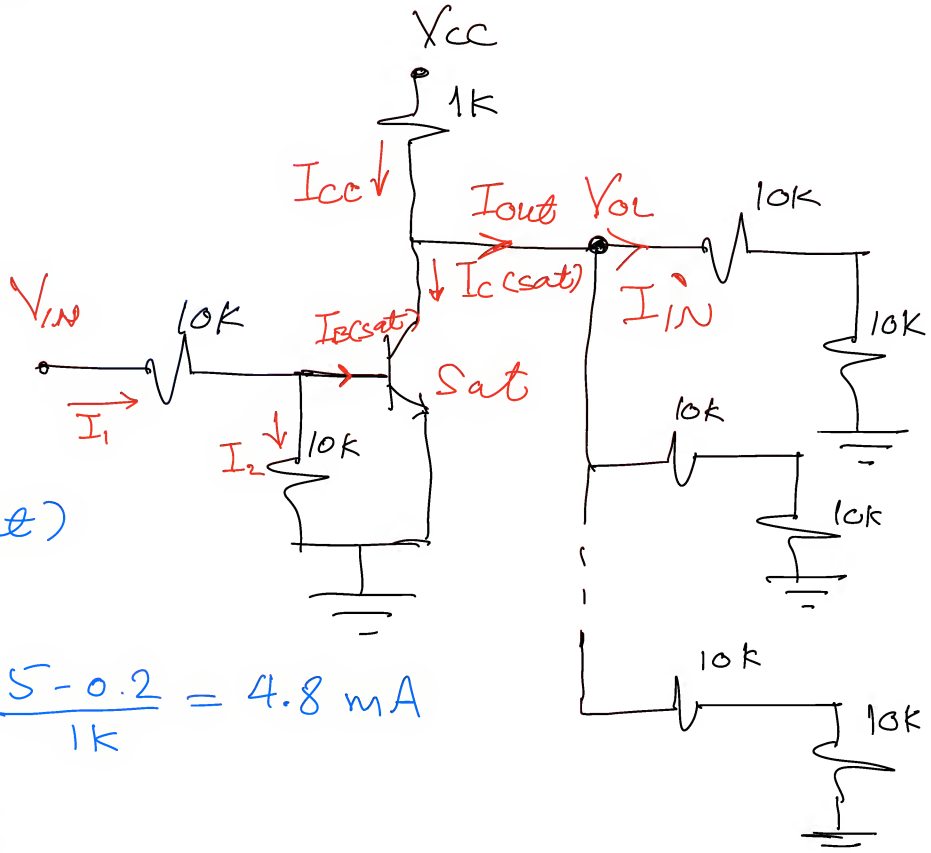


* N_{low}

$I'_{IN} = \frac{V_{OL}}{20K} = \frac{0.2}{20K}$

$I'_{IN} = 0.01\,mA$

$I_{out(low)} = I_{CC} - I_{C(sat)}$



$I_{CC} = \frac{V_{CC} - V_{CE(sat)}}{1K} = \frac{5 - 0.2}{1K} = 4.8\,mA$

$I_{C(sat)} = \beta_F I_{B(sat)}$

$$I_{B(sat)} = I_1 - I_2 = \frac{V_{IN} - V_{BE(sat)}}{10K} - \frac{V_{BE(sat)}}{10K} = \frac{5 - 0.8 \times 2}{10K}$$

$$I_{B(sat)} = 0.34 \text{ mA}$$

$$I_{C(sat)} = 0.5 \times 80 \times 0.34 \text{ m} = 13.6 \text{ mA}$$

$$I_{out(low)} = 4.8\text{m} - 13.6\text{m} = -8.8 \text{ mA}$$

*But $I_{out(low)}$ should never be negative & since it's negative the transistor is not in saturation mode & therefore the output low shouldn't be used to determine N_{max}. thus N_{max} depends only on output high

$$N_{max} = N_{high} = 20$$

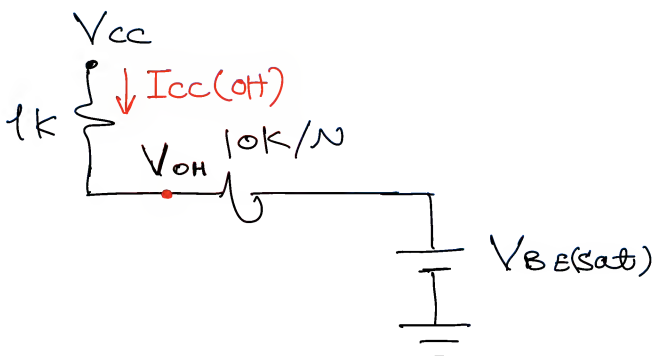
∴ The maximum fan-out is $N = 20$

C $N = 3$

$$P_{D(avg)} = \frac{P_{CC(OH)} + P_{CC(OL)}}{2} = \left(\frac{I_{CC(OH)} + I_{CC(OL)}}{2}\right) V_{CC}$$

$$I_{CC(OH)} = \frac{V_{CC} - V_{BE(sat)}}{1K + \frac{10K}{N}}$$

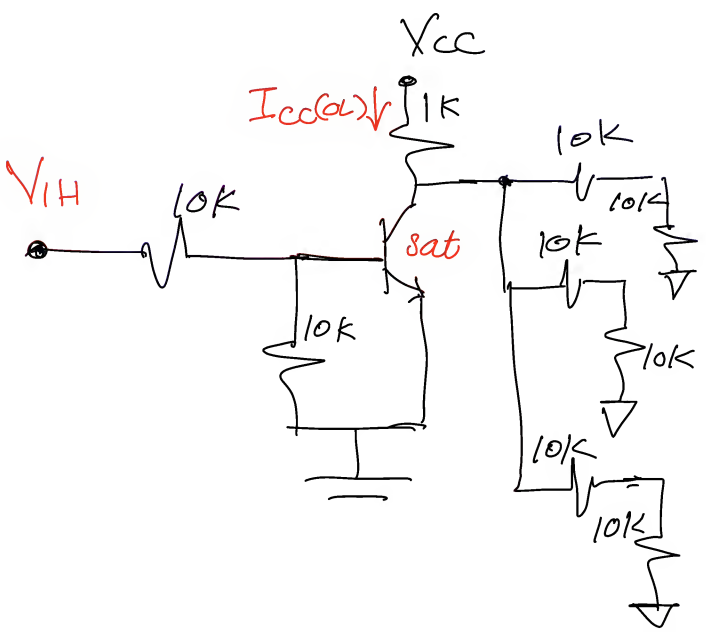
$$I_{CC(OH)} = \frac{5 - 0.8}{1K + \frac{10K}{3}} = 0.969 \text{mA}$$



$$I_{CC(OL)} = \frac{V_{CC} - V_{CE(sat)}}{1K}$$

$$= \frac{5 - 0.2}{1k} = 4.8 \text{mA}$$

$$P_{D(avg)} = \left(\frac{0.969\text{m} + 4.8\text{m}}{2}\right)(5)$$



$$P_{D(avg)} = 14.42 \text{ mW}$$

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